IN THE CLAIMS:

Kindly cancel claim 6 without prejudice.

Kindly amend the claims as follows.

Sub F1

1. (Amended) A substrate bias generator of a semiconductor memory device having a voltage pump circuit to boost a substrate voltage in response to an input of an oscillating signal generated in an oscillator, said substrate bias generator further comprising:

a substrate voltage level detector [for inputting] having said substrate voltage input thereto and outputting a signal which drives said oscillator in response to [said input] a substrate voltage level detected by said substrate voltage level detector, said substrate voltage level detector comprising:

a first MOS transistor having a channel connected to a power supply, said first MOS transistor being operated in response to a level of said substrate voltage, and

a second MOS transistor having a channel connected in series with a channel of said first MOS transistor

and to a ground supply and having a gate connected to said substrate voltage; and

a controller [for inputting] having input thereto a chip active enable signal, a self refresh mode enable signal, and an output signal of said substrate voltage level detector, said controller [and for] controlling a switching operation of said substrate voltage level detector in response to said substrate voltage [input] level detected by said substrate voltage level detector.

Cont'd A11

2. (Amended) A substrate bias generator [as claimed in claim 1,] of a semiconductor memory device having a voltage pump circuit to boost a substrate voltage in response to an input of an oscillating signal generated in an oscillator, said substrate bias generator further comprising:

a substrate voltage level detector having said substrate voltage input thereto and outputting a signal which drives said oscillator in response to a substrate voltage level detected by said substrate voltage level detector, [wherein] said substrate voltage level detector [comprises] comprising:

a first PMOS transistor whose source terminal is coupled to a power supply terminal and whose gate

terminal is coupled to an output signal of said controller, [;]

first resistance means formed between said first PMOS transistor and a predetermined connecting node, [;]

a second PMOS transistor whose source terminal is coupled to said connecting node and whose gate terminal is coupled to said substrate voltage, [;]

second resistance means formed between said second PMOS transistor and a ground voltage terminal, [;] and

an inverter having an input terminal coupled to said connecting node and outputting an output signal of said substrate voltage level detector; and

a controller having input thereto a chip active enable signal, a self refresh mode enable signal, and an output signal of said substrate voltage level detector, said controller controlling a switching operation of said substrate voltage level detector in response to said substrate voltage level detected by said substrate voltage level detector.

3. (Amended) A substrate bias generator [as claimed in] according to claim 2, wherein said controller comprises:

a NOR circuit [inputting a reverse signal] having an input of said chip active enable signal and having input thereto an inversion of said self refresh enable signal [, respectively]; and

an AND circuit [each inputting] having input thereto said output signal of said substrate voltage level detector and [said] an output signal of said NOR circuit, said AND circuit [and then] controlling said first PMOS transistor.

4. (Amended) A substrate bias generator of a semiconductor memory device which performs refresh operations of memory cells according to [said] a self refresh mode for refreshing said memory cells, [by means of] said substrate bias generator comprising:

a voltage pump circuit to supply a negative voltage to a substrate; [,]

an oscillator to drive said voltage pump circuit; [, and]

a substrate voltage level detector to detect a level of said negative voltage and to drive said oscillator in response to said [detecting] detected level; and [, said substrate bias generator comprising:]

a [first logic] controller circuit [inputting] having input thereto a [said] chip active enable signal, a [and said] self refresh mode enable signal, [respectively] and an output of said substrate voltage level detector, an output of said controller circuit being input to said substrate voltage level detector; [a second logic circuit inputting an output signal of said first logic circuit and an output signal of said substrate voltage level detector, respectively;]

said substrate voltage level detector comprising:

a PMOS transistor [whose] having a gate [terminal is] coupled to [an] said output [signal] of said [second logic] controller circuit and [whose] having a source [terminal is] coupled to a power supply terminal, and [thereby]

a MOS transistor having a gate connected to said negative voltage and a channel connected in series with a channel of said PMOS transistor and between said power supply and a ground supply, said MOS transistor being operated in response to a level of said negative voltage,

said PMOS transistor selectively providing power [supply] to said [substrate voltage level detector] MOS

transistor in response to said output signal of said [second logic] controller circuit.

5. (Amended) A substrate bias generator [as claimed in] according to claim 4, wherein said [first logic] controller circuit [is comprised of] comprises:

a NOR circuit; and

an AND circuit connected to an output of said NOR circuit.

Kindly add the following new claim.

--7. A substrate bias generator according to claim 1, wherein said controller comprises:

a NOR circuit having an input of said chip active enable signal and having input thereto an inversion of said self refresh enable signal; and

an AND circuit having input thereto said output signal of said substrate voltage level detector and an output signal of said NOR circuit, said AND circuit controlling said first PMOS transistor.--